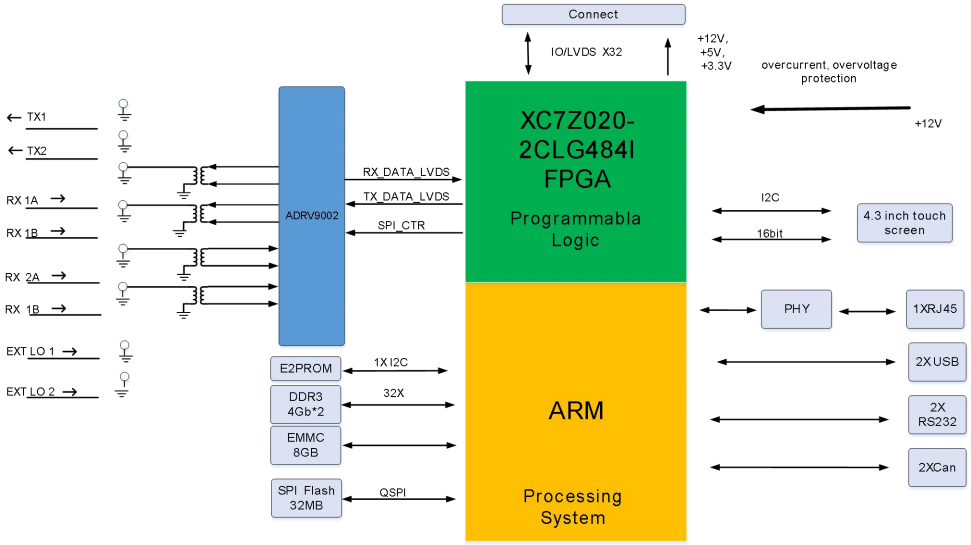
# Software Radio SDR based on ADRV9002 + ZYNQ7020

# (upgrade AD9361)



1. **Overview**

The board is designed by ADI ADRV9002+Xilinx XC7Z020-CLG484 chip, including dual RF input and output channels, supporting gigabit network, RS232, touch screen and other interfaces. Dual-core ARM supports Linux operating system. The board has low power consumption and is suitable for the development of custom wireless protocols, such as Loar, Wifi, 4G platform, etc., as well as the product development of wireless handsets and graphics modules.




2. **Specification**

| Item | Parameters. | Content. |
|---|---|---|
| PS end | ARM | Dual core A9 MPCore, up to 866MHz. |
| | DDR | DDR3 1GB 32bit@800MHz |
| | QSPI Flash | 256Mb |
| | EMMC | 8GB |
| | SD Card | 16GB SD card |
| | RS232 | 2-way RS232 |
| | USB | 1 way USB2.0, 1 way RS232 to USB debug port |
| | The network | 1-way Gigabit RJ45 Ethernet |
| | Touch screen | 4.3 inch touch capacitive screen |
| PL end | Logical resources | 85K Logic Cells，4.9Mb BlockRAM，220 DSP Slices |
| | Extend IO | 32bit LVTTL 3.3V |
| ADRV9002 | Transceiver channel | Double receiving and sending, supporting MiMo |
| | Transceiver bandwidth | Frequency range 30 MHz to 6000MHz;<br>bandwidth 12 kHz to 40 MHz |
| | Digital interface | LVDS and CMOS synchronous serial data interface options |
| | Clock | 32.768MHz TCXO of 0.5ppm |
| | Upgrade AD9361 performance | ● Support for narrowband Transmitter and receiver bandwidth from 12 kHz to 40 MHz<br>● Receiver provides 20dB gain, attenuator prior to the mixer provides 34dB total gain control range in 0.5dB steps<br>● Multi-Chip Synchronization<br>● Automatic Gain Control<br>● Programmable FIR Channel Filters<br>● Fast Frequency Hopping ， Standards as fast as <20us<br><br>Refer to ADRV9002/3/4 Agile, SDR Transceiver Family Introduction documentation |
| Board size | 150mm x 95mm | |
| Power supply | +12V@2A | |

| | |
|---|---|
| Power consumption | 20W |
| Operating temperature | Industrial -20℃ to +70℃ |

**3.Software**

| Item | Parameter | |
|---|---|---|
| Main processor | XC7Z020-2CLG484I | |
| Software version | Vivado2021.2 | |
| programing language | Verilog | |
| PL side test program | ADRV9002 channel interface program | |
| | LED test program | |
| | IO test program | |
| | AXI bus DMA Test Program | |
| | | |
| PS end bare Metal Test Program | DDR3 test program | |
| | Network test program | |
| | RS232 test program | |
| | QSPI Flash test program | |
| | Emmc test program | |
| | SD Card test program | |
| | AXI bus DMA Test Program | |
| PS operating system program | Uboot version | U-Boot 2017.01 |
| | LINUX kernel version | LINUX-4.6.0-g399574f |
| | Serial port software | Xshell6； secureCRT7.0 |

| | | |
|---|---|---|
| | Vivado version | 7z100_vivado2017.4@2017.4 |
| | DDR3 read and write on PS side | |
| | HDMI display | (not available by default) |
| | USB interface test | |
| | Network port test | |
| | Serial port test | |
| | QSPI Flash memory | U16 |
| | SD card starts the test | |
| | EMMC memory | |

**4. Application**

Software radio processing platform